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10/020,848	12/12/2001	Barnes Cooper	ITL.0675US	1071

7590 11/17/2003

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EXAMINER

CABRERA, ZOILA E

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 11/17/2003

5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

10/020,848

Applicant(s)

COOPER, BARNES

Examin r

Zoila E. Cabrera

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4. 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to independent claims 1, 11 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 8, 11-15, 18, 21-25 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by **Kung (US 6,636,910)**.

Claims 1, 11, and 21 are so broad as to read in **Kung**. Regarding claims 1, 11 and 21 **Kung** discloses a method and a system comprising:

- detecting that a processor's frequency has changed in response to processor cooling (Col. 1, lines 55-62); and generating an interrupt in response to the detection of the frequency change (Col. 1, lines 62-67, i.e., The CPU *then* performs a corresponding interrupt processing program to deal with related actions *after* the peripheral processor is reduced to the second operating velocity or second predetermined frequency).

As for claims 2-5, 8, 12-15, 18, 22-25, and 28, **Kung** further discloses,

- providing an interrupt to an operating system (Col. 1, lines 64-67);
- reading the performance state of the processor in response to the interrupt (Col. 2, lines 61-67);
- determining a new performance state (Col. 3, lines 63-67 – Col. 4, lines 1-2);
- scheduling a bandwidth allocation (Col. 2, lines 52-56; Col. 3, lines 6-10 and lines 38-41);
- detecting a high temperature or a low temperature interrupt and reading the processor performance state in response to the detection of a high temperature or a low temperature interrupt (Col. 2, lines 61-67; Col. 1, lines 62-67; Col. 3, lines 1-10 and lines 63-67; Col. 4, lines 1-2);

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-7, 10, 16-17, 20, 26-27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kung** as applied to claims 1, 11 and 21 above, and further in view of **Inoue (EP 1085399 A1)**.

Kung discloses the limitations of claims 1, 11, and 21 above but fail to specifically disclose the limitations of claims 6-7, 16-17, 26-27. However, **Inoue** discloses such limitations as follows:

- setting up a periodic timer (Fig. 3, element 25);
- monitoring the processor temperature at periodic intervals (Fig. 4, and 7, step S1; Figs. 6 and 8, Step T1);
- using hardware controlled throttling (Col. 9, lines 46-49).

Therefore, it would have been obvious to a person of the ordinary skill in the art at the time the invention was made to combine the teachings of **Kung** with **Inoue** because It would provide with an improved temperature controller that efficiently monitors the temperature of an electronic apparatus by periodically monitoring the status of the device.

Claims 9, 19 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kung** as applied to claims 1, 11 and 21 above, and further in view of **Moriyama** (US 6,510,400).

Kung discloses the limitations of claims 1, 11, and 21 above but fail to specifically disclose, regarding claims 9, 19 and 29, detecting a frequency change includes detecting a processor phase locked loop event. However, **Moriyama** discloses detecting a processor phase locked loop event (Col. 5, lines 6-10). Therefore, it would have been obvious to a person of the ordinary skill in the art at the time the invention

Art Unit: 2125

was made to combine the teachings of **Kung** with **Moriyama** because it would provide with a SWEEP function for gradually varying the clock frequency (Col. 5, lines 7-11).

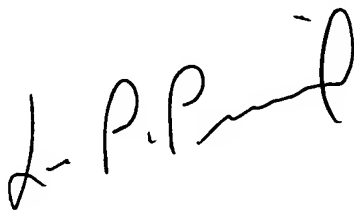
Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning communication or earlier communication from the examiner should be directed to Zoila Cabrera, whose telephone number is (703) 306-4768. The examiner can normally be reached on M-F from 8:00 a.m. to 5:30 p.m. EST (every other Friday).

If attempts to reach the examiner by phone fail, the examiner's supervisor, Leo Picard, can be reached on (703) 308-0538. Additionally, the fax phones for Art Unit 2125 are (703) 308-6306 or 308-6296. Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist at (703) 305-9600.

Zoila Cabrera
Patent Examiner
11/12/03

A handwritten signature in black ink, appearing to read 'L. Picard', with a stylized flourish at the end.

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100



US006636910B2

(12) **United States Patent**
Kung et al.

(10) **Patent No.:** US 6,636,910 B2
(45) **Date of Patent:** Oct. 21, 2003

(54) **PERIPHERAL DEVICE OF A PORTABLE COMPUTER WITH THERMAL CONTROL CIRCUITRY**

5,745,375 A * 4/1998 Reinhardt et al. 700/286
6,192,479 B1 * 2/2001 Ko 713/300
6,397,343 B1 * 5/2002 Williams et al. 713/501

(75) **Inventors:** Shao-Tsu Kung, Taipei (TW);
Jenq-Haur Pan, Taipei (TW)

* cited by examiner

(73) **Assignee:** Compal Electronics, Inc., Taipei (TW)

Primary Examiner—Kim Huynh

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 46 days.

(74) *Attorney, Agent, or Firm*—Winston Hsu

(21) **Appl. No.:** 09/683,134

(22) **Filed:** Nov. 25, 2001

(65) **Prior Publication Data**

US 2002/0194402 A1 Dec. 19, 2002

(30) **Foreign Application Priority Data**

Jun. 15, 2001 (TW) 90114512 A

(51) **Int. Cl.⁷** G06F 1/08; G06F 3/00

(52) **U.S. Cl.** 710/60; 710/48; 713/501

(58) **Field of Search** 710/48, 36, 58,
710/60; 713/322–324, 600, 501; 361/103,
93.2, 93.8; 700/46; 714/47; 340/825.71,
825.73; 702/132

(56) **References Cited**

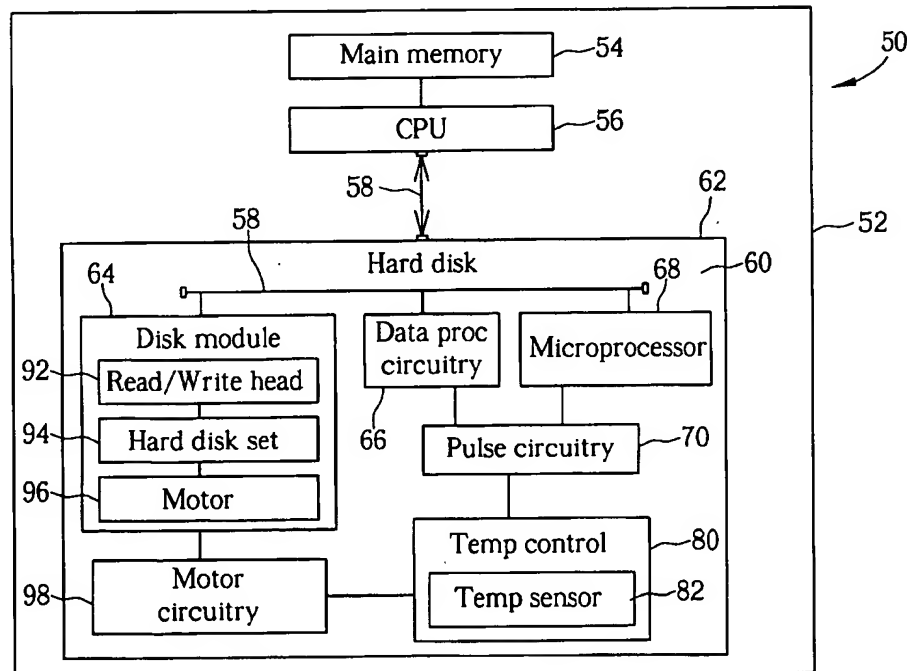
U.S. PATENT DOCUMENTS

5,490,059 A * 2/1996 Mahalingaiah et al. 700/46

(57) **ABSTRACT**

A peripheral device with thermal control circuitry is set within a casing of a portable computer. The peripheral device includes at least a peripheral processor set for providing specific operations, and pulse circuitry electrically connected to the peripheral processor for producing pulse signals with a predetermined first frequency and transmitting to the peripheral processor. The pulses are used so that the peripheral processor can operate according to a predetermined first operation velocity. The peripheral device also includes thermal control circuitry with a thermal sensor. When a temperature detected by the thermal sensor exceeds a first predetermined temperature, the thermal control circuitry produces a first output to the pulse circuitry so as to reduce the frequency of the pulse signals to a predetermined second frequency. This reduces the operating velocity of the peripheral processor to a second operating velocity.

4 Claims, 2 Drawing Sheets



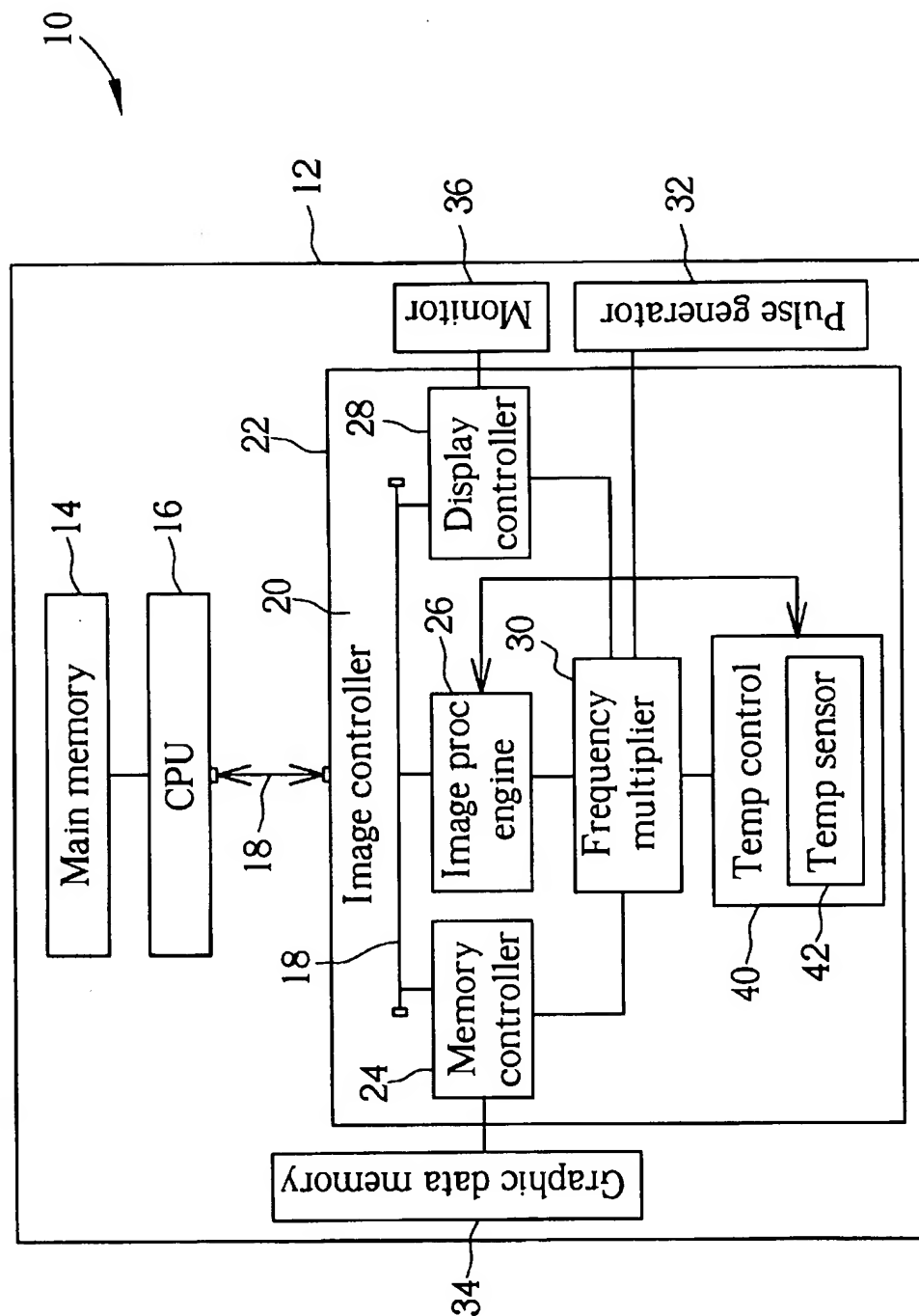


Fig. 1

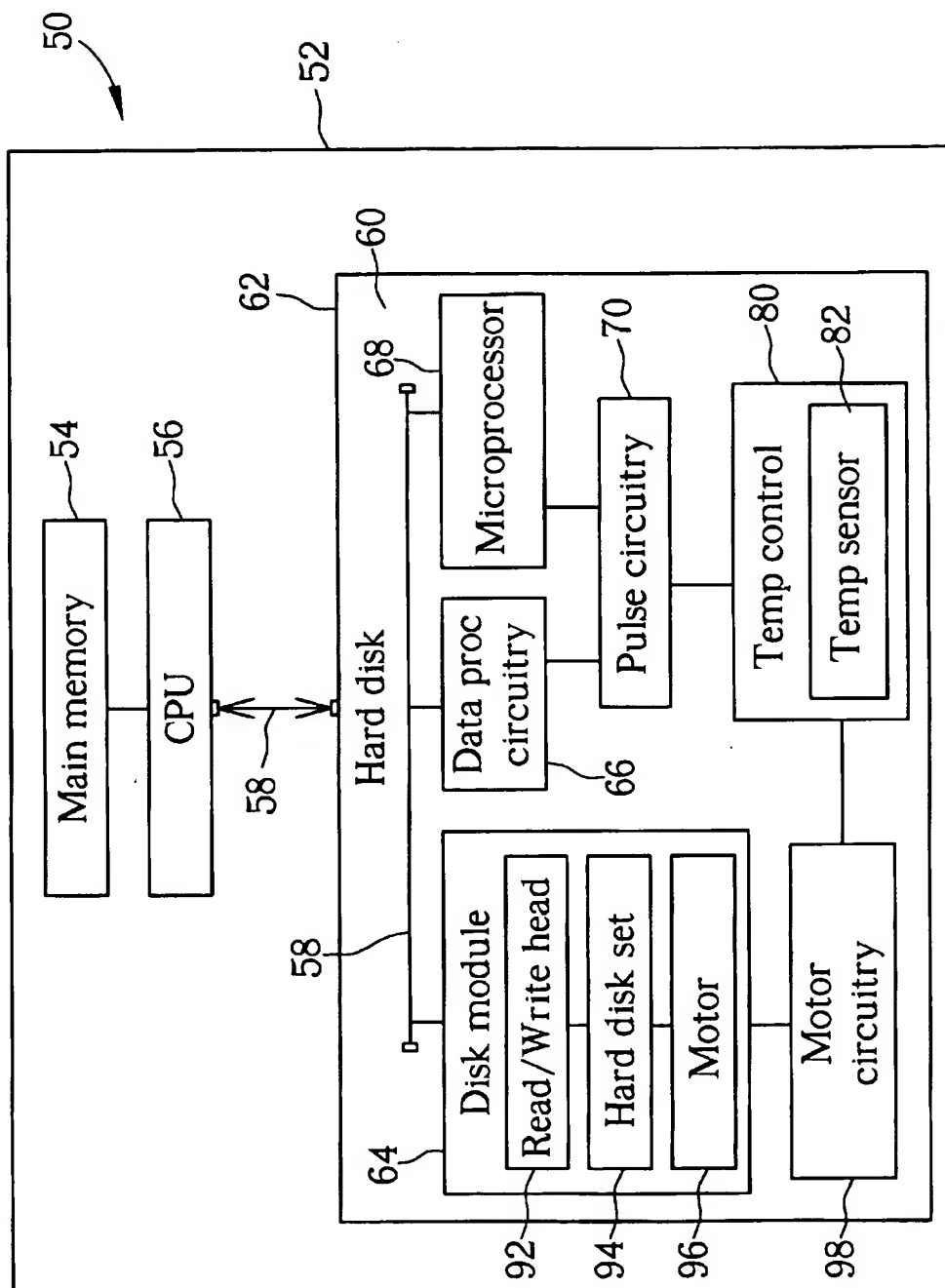


Fig. 2

1

PERIPHERAL DEVICE OF A PORTABLE COMPUTER WITH THERMAL CONTROL CIRCUITRY

BACKGROUND OF INVENTION

1. Field of the Invention

The present invention relates to a peripheral device of a portable computer, and more particularly to a peripheral device of a portable computer with thermal control circuitry.

2. Description of the Prior Art

With the quick development of information technology, computer systems widely used in every industry are playing an important role in many companies for modernization. The manufacturing of portable computers has become a mainstream business in the computer industry because of the increase of data storage density, the improvement of operational speed, and the decrease of production cost.

When designing portable computers, the problem of expelling heat is one of the most important factors to consider. In general, the source of heat mostly comes from the central processing unit (CPU). Therefore, heat dissipation systems in portable computers are mainly designed to expel the heat generated from the CPU. Along with the improvements of the system performance brought by increasing the operational speed of the CPU, the temperature of PC components and the computer system also increase. A poorly designed heat dissipation system may make the system unstable for high temperatures. It may hurt users due to the overheated system and PC components. Unfortunately, the phenomenon is not likely to be observed by users while using computers. When the temperature reaches the maximum tolerable level, the system will become unstable.

SUMMARY OF INVENTION

A peripheral device with thermal control circuitry is set within a casing of a portable computer. The portable computer further includes a main memory for storing programs and data, a central processing unit (CPU) for executing programs stored in the main memory, and a bus for connecting the peripheral device and the CPU. The peripheral device includes an outer package for protecting inner components of the peripheral device, and at least a peripheral processor set within the outer package for providing a specific operation, control, or driving functions. The peripheral device further includes pulse circuitry set within the outer package and electrically connected to the peripheral processor. The pulse circuitry produces pulse signals with a predetermined first frequency and transmits the signals to the peripheral processor, so that the peripheral processor can operate according to a predetermined first operation velocity, and thermal control circuitry set within the outer package with a thermal sensor. When a temperature detected by the thermal sensor of the thermal control circuitry exceeds a first predetermined temperature, the thermal control circuitry produces a first output to the pulse circuitry. This first output reduces the frequency of the pulse signals to a predetermined second frequency, so that the operating velocity of the peripheral processor is reduced to a second operating velocity. Simultaneously, the thermal control circuitry produces an interrupt signal to interrupt operation of the CPU. The CPU then performs a corresponding interrupt processing program to deal with related actions after the peripheral processor is reduced to the second operating velocity.

2

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of the first embodiment of a portable computer according to the present invention.

FIG. 2 is a block diagram of the second embodiment of a portable computer according to the present invention.

DETAILED DESCRIPTION

Please refer to FIG. 1, which is a block diagram of the first embodiment of a portable computer 10 according to the present invention. As shown in FIG. 1, the portable computer 10 comprises a main memory 14 for storing programs and data, a central processing unit (CPU) 16 for executing programs stored in the main memory 14, a peripheral device 20 installed inside a housing 12 of a portable computer 10, and a bus 18 for connecting the peripheral device 20 and the CPU 16.

In the present embodiment, the peripheral device 20 is an image controller 20 comprising an external housing 22 for protecting internal components of the image controller 20, a memory controller 24 electronically connected between an external graphic data memory 34 and the bus 18 for controlling reading and writing of graphic data in the graphic data memory 34, a display controller 28 for controlling image displays of an external monitor, and an image processing engine 26 for processing graphic data in the graphic data memory 34 and transmitting the graphic data to the display controller 28. The peripheral device 20 also includes a frequency multiplier 30, electronically connected to the memory controller 24 and the image processing engine 26, for generating the first predetermined frequency of pulses, and for transmitting the pulses to the memory controller 24 and the image processing controller 20 operated according to the first predetermined speed. The peripheral device 20 also includes temperature control circuitry 40 installed inside the housing 22 having a temperature sensor 42 for detecting the surrounding temperature of the image controller 20. Furthermore, the frequency multiplier 30, which is electronically connected to an external pulse generator 32, changes the frequency of pulses transmitted from the external pulse generator 32.

When the temperature detected by the temperature sensor 42 of the temperature controlled circuitry 40 exceeds a predetermined level, the temperature controlled circuitry 40 generates the first request to the frequency multiplier 30. Then, the frequency multiplier 30 reduces the frequency of pulses generated by the external pulse generator 32 to the second predetermined frequency so as to reduce the speed of both the memory controller 24 and the image processing engine 26 to the second predetermined speed. Meanwhile, the temperature controlled circuitry 40 transmits the first request to the image processing engine 26 for adjusting the image processing engine 26 to the second predetermined speed, according to the pulse signal generated by the frequency multiplier 30. Simultaneously, the temperature controlled circuitry 40 generates an interrupt signal to interrupt the operation of the CPU 16, and the CPU 16 executes a corresponding interrupt processing program. This program handles the operation of the memory controller 24, the image processing engine 26, and the display controller 28 after decreasing the operation speed.

When the temperature detected by the temperature sensor 42 of the temperature controlled circuitry 40 is lower than the first predetermined temperature, it means that the CPU 16, the memory controller 24, the image processing engine 26, and the display controller 28 operate too slowly. Therefore, it is necessary to increase the operational speed for achieving the maximum performance. The temperature controlled circuitry 40 generates the second request to the frequency multiplier 30 for increasing the frequency generated by the frequency multiplier 30 to the first predetermined frequency. Then the memory controller 24, the image processing engine 26, and the display controller 28 operate at the first predetermined speed. Using the temperature sensor 42 of the temperature controlled circuitry 40 to adjust the frequency of pulse signals generated from the frequency multiplier 30 thereby maintains the stability of internal components and the whole system.

Please refer to FIG. 2, which is a block diagram of the second embodiment of a portable computer according to the present invention. As shown in FIG. 2, the portable computer 50 comprises a main memory 54 for storing programs and data, a central processing unit (CPU) 56 for executing programs stored in the main memory 54, a peripheral device 60 installed inside a housing 52 of a portable computer 50, and a bus 58 for connecting the peripheral device 60 and the CPU 56.

In the present embodiment, the peripheral device 60 is a hard disk comprising a housing 62, a disk module 64, data process circuitry 66, a microprocessor 68, motor driving circuitry 98, pulse circuitry 70, and temperature controlled circuitry 80. The housing 62 is used to protect the internal components. The disk module 64 comprises a hard disk set 94 for storing data, a read/write head 92 for writing data into the hard disk set 94 or retrieving data from the hard disk set 94, and a motor 96 for driving the hard disk set 94. The data process circuitry 66 is electronically connected to the read/write head 92 of the disk module 64 and the bus 58 for processing data stored in the disk module 64 or data retrieved from the disk module 64. The microprocessor 68 is used for controlling operations of the hard disk drive 60. The motor driving circuitry 98 is used for controlling the rotations of the motor 96 of the hard disk set 64. The pulse circuitry 70 is electronically connected to the data process circuitry 66 and the microprocessor 68 for controlling the speed of the data process circuitry 66 and the microprocessor 68. The temperature controlled circuitry 80 installed inside the housing 62 comprises a temperature sensor 82 for detecting the temperature of the surroundings when the hard disk 60 is operating.

When the temperature detected by the temperature sensor 82 of the temperature controlled circuitry 80 exceeds the first predetermined level, the temperature-controlled circuitry 80 will generate the first request to the pulse circuitry 70. Then, the pulse circuitry 70 decreases the frequency of pulses generated by the pulse circuitry 70 to the second predetermined frequency so as to reduce the speed of the data process circuitry 66 and the speed of the microprocessor 68 to the second predetermined speed. Meanwhile, the temperature controlled circuitry 80 will generate another request to the motor driving circuitry 98 so that the motor driving circuitry 98 will reduce the rotational speed of the motor 96 of the hard disk module 64.

When the temperature detected by the temperature sensor 82 of the temperature controlled circuitry 80 is lower than the first predetermined temperature, it means that the CPU 56, the hard disk module 64, the data process circuitry 66, and the microprocessor 68 operate too slowly. Therefore, it

is necessary to increase the operational speed for achieving maximum performance. The temperature controlled circuitry 40 generates a second request to the pulse circuitry 70 for increasing the frequency generated by the pulse circuitry 70 to the first predetermined frequency. Then the hard disk module 64, the data process circuitry 66, and the microprocessor 68 operate at the first predetermined speed. Using the temperature sensor 82 of the temperature controlled circuitry 80 to detect the surrounding temperature of the hard disk 60 for adjusting the frequency of pulses generated from the pulse circuitry 70 thereby maintains the stability of internal components of external devices and the whole system.

The above disclosure is not intended as limiting. Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A hard disc drive installed inside a housing of a portable computer, the portable computer comprising a main memory for storing programs and data, a central processing unit for executing programs stored in the main memory, and a bus for connecting the peripheral device and the central processing unit, the hard disc drive comprising:

a housing for protecting elements inside the hard disc drive;

a disc module installed inside the housing and having a hard disc set for storing data, a read/write head for writing data into the hard disc set or retrieving data from the hard disc set, and a motor for driving the hard disc set;

data process circuitry installed inside the housing and electrically connected to the read/write head of the disc module and the bus for processing data stored in the disc module or data retrieved from the disc module;

a microprocessor installed inside the housing for controlling operations of the hard disc drive;

pulse circuitry installed inside the housing and electrically connected to the data process circuitry and the microprocessor for controlling the speed of the data process circuitry and the speed of the microprocessor; and

temperature controlled circuitry installed inside the housing having a temperature sensor;

wherein when a temperature detected by the temperature sensor exceeds a first predetermined level, the temperature controlled circuitry will generate a first request to the pulse circuitry to reduce a frequency of pulses generated by the pulse circuitry from a first frequency to a second frequency so as to reduce a speed of the data process circuitry and the speed of the microprocessor from a first speed to a second speed.

2. The hard disc drive of claim 1 wherein when the temperature detected by the temperature sensor exceeds the first predetermined level, the temperature controlled circuitry will generate an interrupt signal to interrupt operations of the central processing unit and execute a corresponding interrupt program to process operations relevant to a reduction of the speed of the data process circuitry and the speed of the microprocessor.

3. The hard disc drive of claim 1 further comprising motor driving circuitry for controlling rotations of the motor; wherein when the temperature detected by the temperature sensor exceeds the first predetermined level, the temperature controlled circuitry will generate another request to the

5

motor driving circuitry so that the motor driving circuitry will reduce a rotational speed of the motor.

4. The hard disc drive of claim 1 wherein when the temperature detected by the temperature sensor is below a second predetermined level, the temperature controlled circuitry will generate a second request to the pulse circuitry to

6

increase the frequency of pulses generated by the pulse circuitry to the first frequency so as to bring the speed of the data process circuitry and the speed of the microprocessor back to the first speed.

* * * * *